INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4001UB
gates
Quadruple 2-input NOR gate

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Quadruple 2-input NOR gate

HEF4001UB gates

DESCRIPTION

The HEF4001UB is a quadruple 2-input NOR gate. This unbuffered single stage version provides a direct implementation of the NOR function. The output impedance and output transition time depends on the input voltage and input rise and fall times applied.

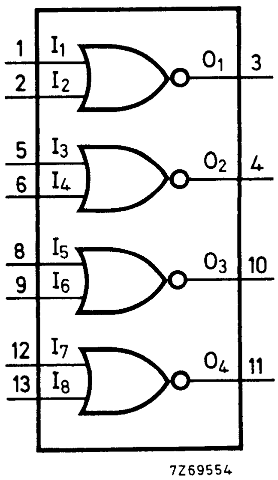

Fig.1 Functional diagram.

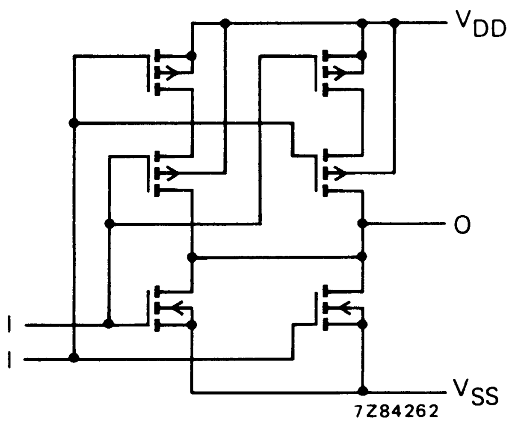

Fig.3 Schematic diagram (one gate). The splitting-up of the p-transistors provide identical inputs.

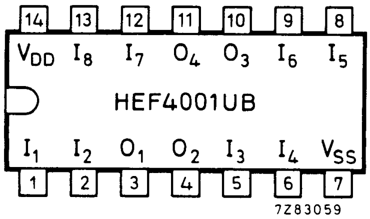

Fig.2 Pinning diagram.

HEF4001UBP(N): 14-lead DIL; plastic (SOT27-1)

HEF4001UBD(F): 14-lead DIL; ceramic (cerdip) (SOT73)

HEF4001UBT(D): 14-lead SO; plastic (SOT108-1)

( ): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications for V_{IH}/V_{IL} unbuffered stages

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
$I_n \rightarrow O_n$	5		65	130	ns	30 ns + (0,70 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	30	60	ns	17 ns + (0,27 ns/pF) C_L
	15		25	50	ns	15 ns + (0,20 ns/pF) C_L
	5		40	80	ns	13 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
Output transition times	5		75	150	ns	15 ns + (1,20 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	6 ns + (0,48 ns/pF) C_L
	15		20	40	ns	4 ns + (0,32 ns/pF) C_L
	5		60	110	ns	10 ns + (1,00 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
Input capacitance		C_{IN}	–	10	pF	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	$500\ f_i + \sum (f_oC_L) \times V_{DD}^2$	where
dissipation per	10	$5000\ f_i + \sum (f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)	15	$30\ 000\ f_i + \sum (f_oC_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum(f_oC_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

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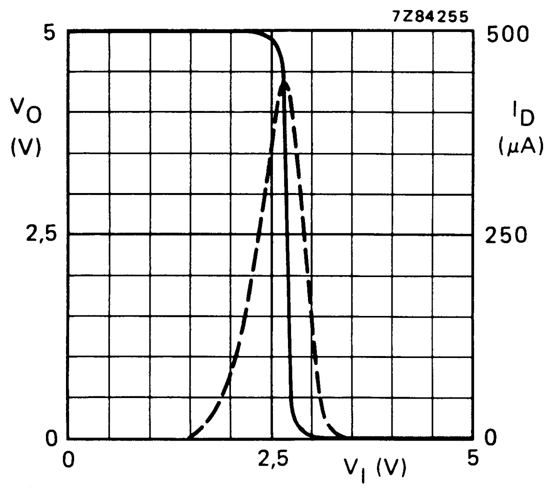


Fig.4 Typical transfer characteristics; one input, the other input connected to V_{SS};
—— V_O;
– – – I_D (drain current);
$I_O = 0$; $V_{DD} = 5$ V.

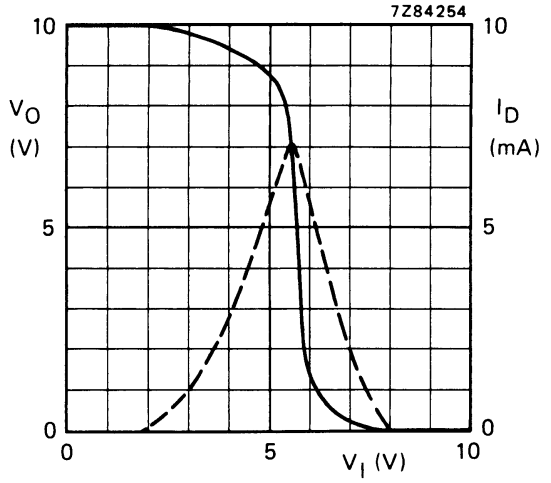


Fig.5 Typical transfer characteristics; one input, the other input connected to V_{SS};
—— V_O;
– – – I_D (drain current);
$I_O = 0$; $V_{DD} = 10$ V.

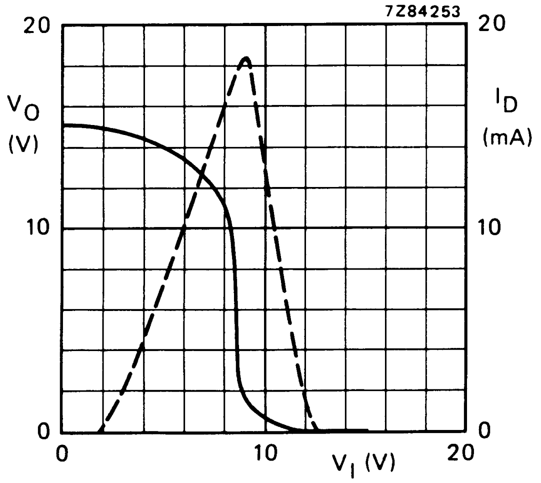


Fig.6 Typical transfer characteristics; one input, the other input connected to V_{SS};
—— V_O;
– – – I_D (drain current);
$I_O = 0$; $V_{DD} = 15$ V.

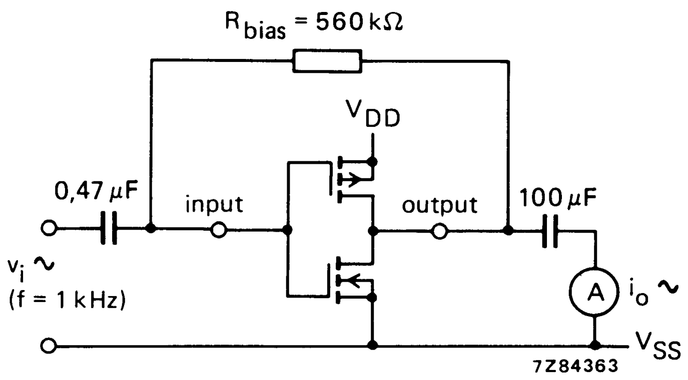
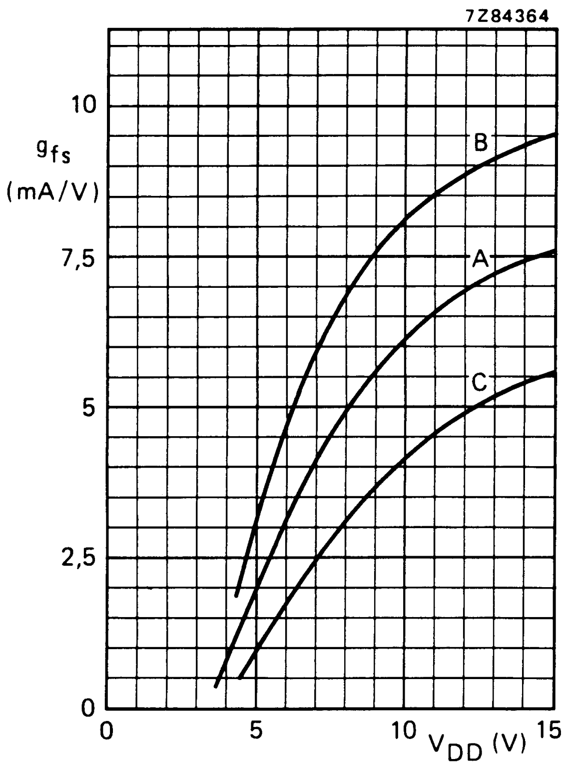


Fig.7 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig.8).

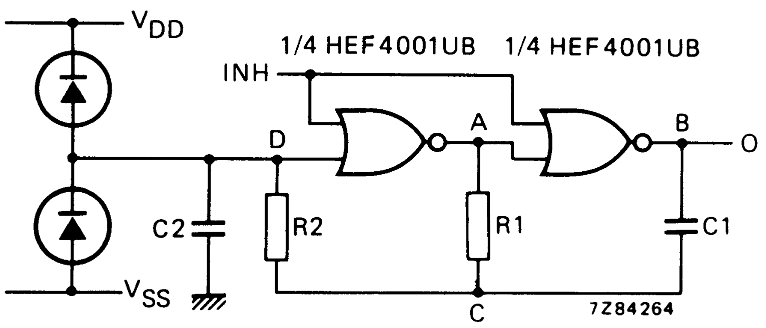


A : average,
B : average + 2 s,
C : average – 2 s, in where ‘s’ is the observed standard deviation.

Fig.8 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.

APPLICATION INFORMATION

Some examples of applications for the HEF4001UB are shown below. Because of the fact that this circuit is unbuffered, it is suitable for use in (partly) analogue circuits.



(a)

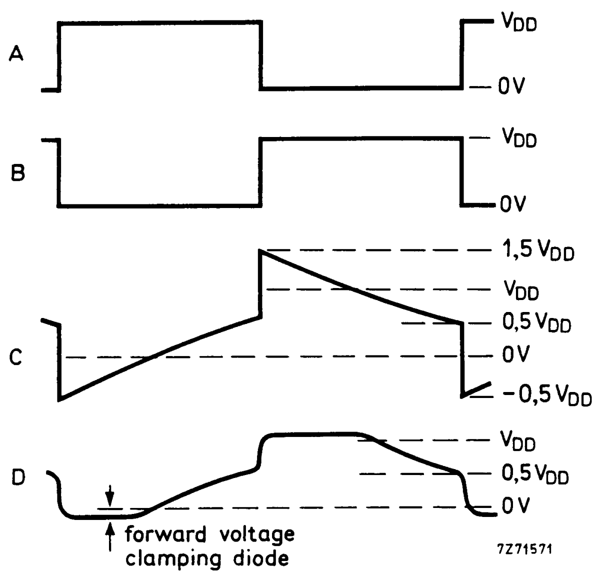
INH	O
H	L
L	OSC

In Fig.9 the oscillation frequency is mainly determined by R1C1, provided R1 << R2 and R2C2 << R1C1.

The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance. The period T_p is given by $T_p = T_1 + T_2$, in which

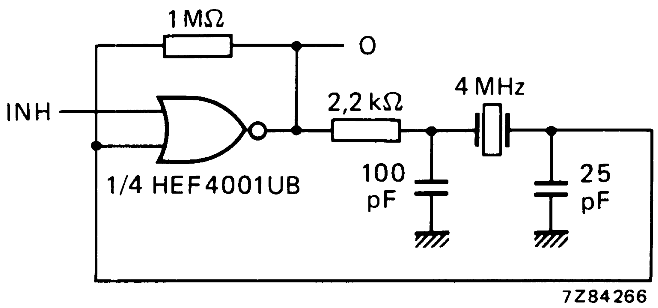
$$T_1 = R1C1 \ln\frac{V_{DD} + V_{ST}}{V_{ST}} \text{ and } T_2 = R1C1 \ln\frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}} \text{ where}$$

V_{ST} is the signal threshold level of the gate. The period is fairly independent of V_{DD}, V_{ST} and temperature. The duty factor, however, is influenced by V_{ST}.



(b)

Fig.9 (a) Astable relaxation oscillator using two HEF4001UB gates; the diodes may be BAW62; C2 is a parasitic capacitance.
(b) Waveforms at the points marked A, B, C and D in the circuit diagram.



INH	O
H	L
L	OSC

Fig.10 Example of a crystal oscillator using one HEF4001UB gate.

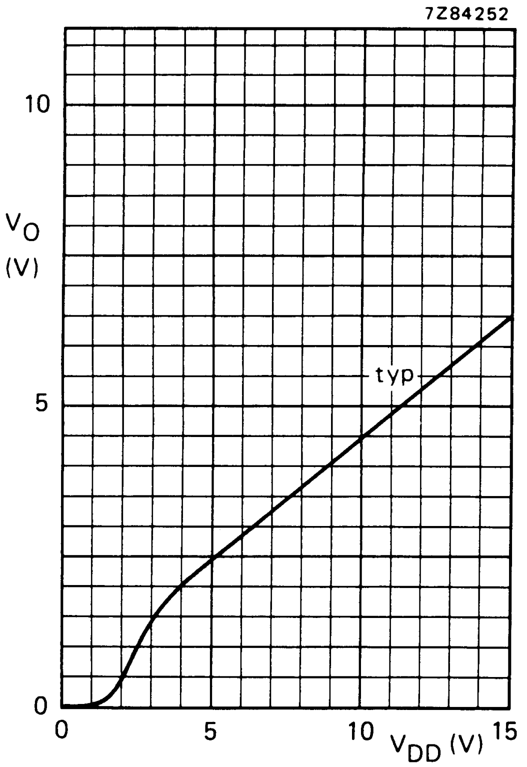


Fig.11 Output voltages as a function of supply voltage.

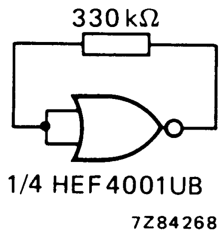


Fig.12 Test set-up for measuring graph of Fig.11. Condition: all other inputs connected to ground.

NOTES

If a gate is just used as an amplifying inverter, there are two possibilities:

1. Connecting the inputs together gives simpler wiring, but makes the device output not completely symmetrical.
2. Connecting one input to V_{SS} will give the device a symmetrical output.

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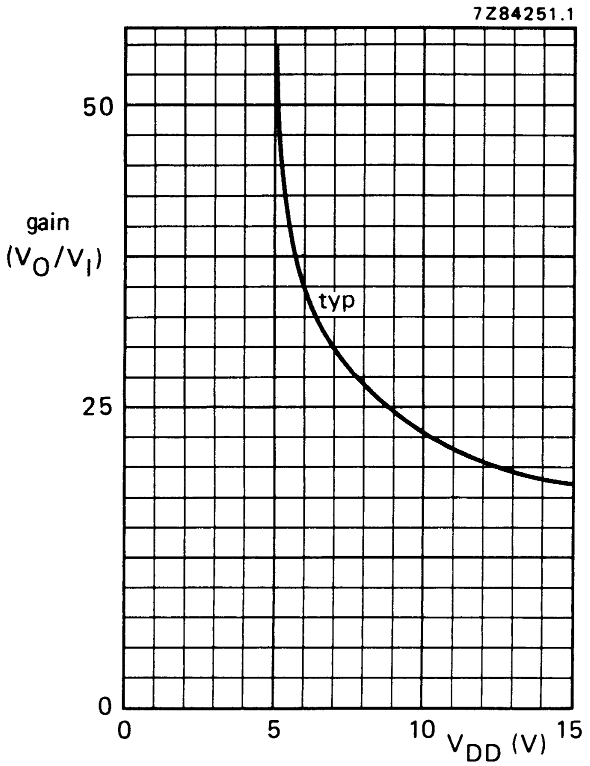

Fig.13 Voltage gain (V_O/V_I) as a function of supply voltage.

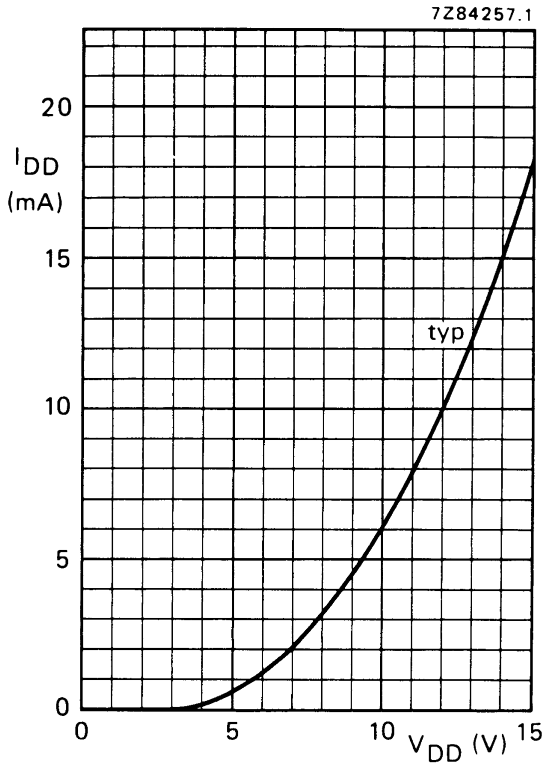

Fig.14 Supply current as a function of supply voltage.

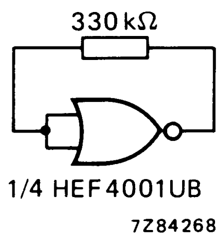

Fig.15 Test set-up for measuring graphs of Figs 13 and 14. Condition: all other inputs connected to ground.

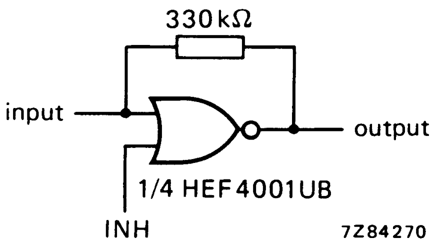

Fig.16 Example of an analogue amplifier with inhibit using one HEF4001UB gate.